A Single Supply High Performance PA MMIC for GSM Handsets using Quasi-Enhancement Mode PHEMT

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Abstract **- A 3-stage GaAs FET power amplifier MMIC utilizing a quasi-enhancement mode PHEMT process has been developed for single supply GSM applications. The MMIC operates from a 3.2V power supply and at 900 MHz, provides 35.5 dBm output power and 63.0% power added efficiency. Another 3 stage MMIC designed for DCS-1800, which at 1750 MHZ provides 33.2 dBm output power with 61.1% PAE, is also presented.**

I. Introduction

The global demand for digital handsets is continuing to grow with the GSM market remaining strong. The requirements for this system are low cost, low operating voltage, high efficiency and dualband operation. To illustrate the potential of this quasi-enhancement mode PHEMT technology, two single supply, separately packaged power amplifier MMICs are demonstrated for GSM and DCS-1800 applications. A previous paper [1] demonstrated the CDMA and TDMA linearity potential for this technology.

II. Device

This technology was used to realize a high power density to minimize chip size, no negative gate bias and high efficiency. This process has a power added efficiency and power density improvement over a previously reported technology [2]. High drain-source current, Ifmax = 360 mA/mm, is obtained typically with +0.1 V threshold voltage, which eliminates a negative gate voltage requirement from handsets. The high transconductance, gm = 460 mS/mm, has been obtained to realize high gain. This PHEMT device also has low drain-source on-resistance which realized high-efficiency at low voltage. Breakdown voltage, Vgdo, is typically +15 V. This is in excess of three times the operating voltage, which may be required under extreme output load conditions.

This process features 0.4 um WSi/Au Schottky gates and a substrate thickness of 28 um with a 30um gold plated backside and a dry backside via process. The thin substrate makes it possible to shrink the PHEMT gate-to-gate pitch, due to the low thermal resistance. This narrow pitch enables the reduction of the chip significantly. Silicon Nitride MIM capacitors, multi-level gold spiral inductors, and epitaxial resistors complete the passive portion of this MMIC process.

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Figure 1 shows the DC-IV characteristics for a Vgs from 0.1 to 0.8V in a 0.1V step. Figure 2 shows the Pin vs Pout and PAE at 900 MHZ for a single stage GSM size output FET. The total gate width is 50mm. At a drain voltage of 3.2V, the small signal gain is 16.7dB, Psat is 36.5 dBm with an associated gain of 12.5 dB and PAE=73.8%. Figure 3 shows the performance at 1750 MHz for a single stage DCS-1800 size output FET. The total gate width is 36mm. At Vd=3.2V, the small signal gain is 13.2 dB, Psat is 33.0 dBm with an associated gain of 10.0 dB and PAE=71.0%.

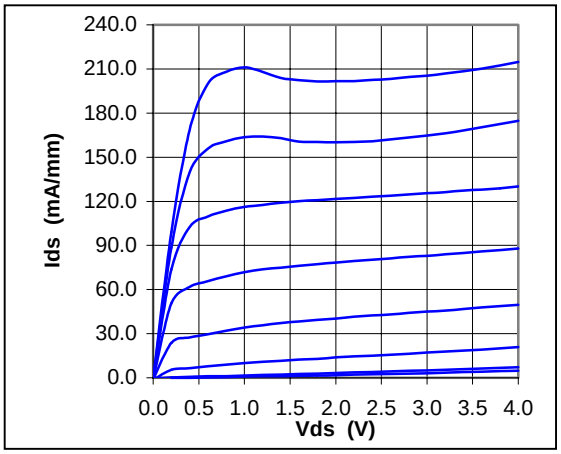

Figure 1. IV characteristics. Vgs=0.1 to 0.8V, 0.1V step

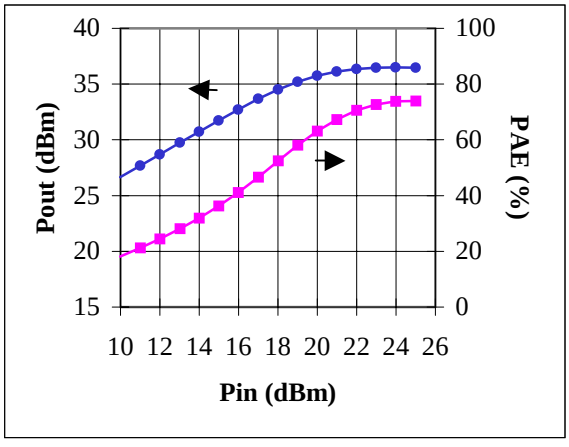

Figure 2. 50 mm FET Performance at 900 MHz
Psat=36.5 dBm, PAE=73.8%

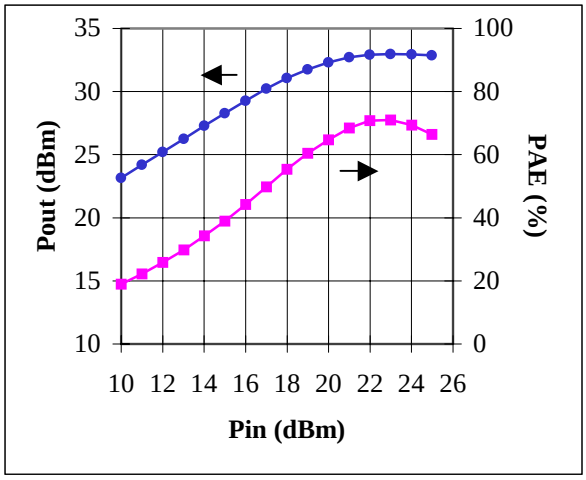

Figure 3. 36mm FET Performance at 1750 MHz
Psat=33.0 dBm, PAE=71.0%

III. Design

FET load pull results were used as the basis for determining the output loading for each stage. A temperature dependent Advanced Curtice nonlinear model, based on IV curves and s-parameters and correlated with measured load pull results, was used to verify the large signal performance.

The three stage GSM MMIC gate widths of the FETs are 1mm, 6mm, 50mm for the 1st 2nd and 3rd stages respectively. The circuit schematic is shown in Figure 4. Being quasi-enhancement mode, the output power cannot be completely shut off under high input drive level when Vgs=0V, which is a GSM requirement, so an input attenuator was needed. A shunt FET attenuator configuration was selected to minimize insertion loss at the low attenuation state to help minimize noise figure and noise power. The gate of the attenuator was set to a fixed reference voltage while the drain and source were connected to Vcontrol. The source has an rf bypass cap to ground. This gives low attenuation at Vcontrol=1.8V and high attenuation as Vcontrol approaches 0V.

The MMIC was designed taking into account the PCB effects on overall performance. The MMIC package typically mounts to the top surface of a printed circuit board with vias going to a lower level ground plane. These vias create a common inductance,

which can generate instability due to source rf current flowing between the 1st stage and 2nd + 3rd stages. The input attenuator and 1st stage grounding are connected to the ground plane through a bond wire from the MMIC to the package pin then to a PCB via separate from the main PCB vias. This provides the isolation needed for stability under high common inductance conditions.

An external cap is used between the 2nd and 3rd stages to fine-tune the interstage match. The output match uses an external shunt C-series transmission line -shunt C. The C's were chosen to simultaneously provide the proper fundamental frequency impedance and a short at the second harmonic through the self-resonance of the capacitors. The chip size is 1.36 mm x 1.5 mm. The mmic is shown in Figure 5.

The DCS-1800 MMIC has a similar configuration as the GSM MMIC. The FET gate widths for the DCS-1800 1st, 2nd and 3rd stages are 1mm, 6mm, and 36mm respectively. The chip size is 1.2 mm x 1.4 mm. The mmic layout is shown in Figure 6.

The package used is a 20 pin 4mm x 4mm x 0.9mm quad leadless plastic package and is shown in figure 7.

IV. Results

Results for the GSM MMIC are shown in figure 8. At 900 MHz, Pin=5dBm and Vdd=3.2V, a Pout of 35.5 dBm was obtained with a 63.0% PAE. The power is controlled by simultaneously increasing the attenuator attenuation and biasing off the gate voltages of the 3 stages using the Vcon voltage. The output power was controllable down to –32 dBm. The 2nd harmonic is –14.6 dBm and the 3rd harmonic is –17.2 dBm at the high power level.

Results for the DCS-1800 MMIC are shown in figure 9. At 1750 MHz, Pin=5dBm and Vdd=3.2V, a Pout of 33.2 dBm was obtained with a 61.1% PAE. The output power was controllable down to –16 dBm. The 2nd harmonic is –13.2 dBm and the 3rd harmonic is –20.0 dBm at the high power level. The Ids leakage current for no rf and Vcon=0V is 1.2 mA for GSM and 0.8 mA for DCS.

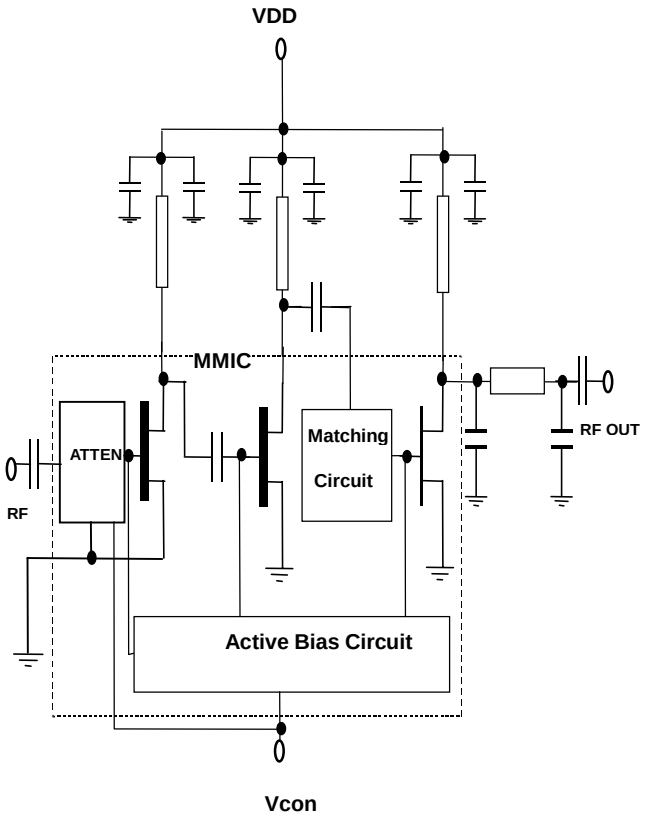

Figure 4. GSM Circuit Diagram

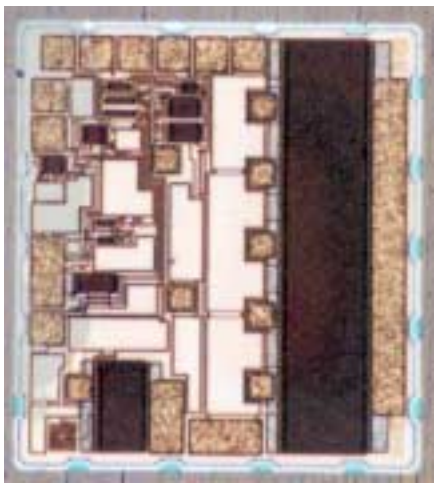

Figure 5. GSM MMIC Layout

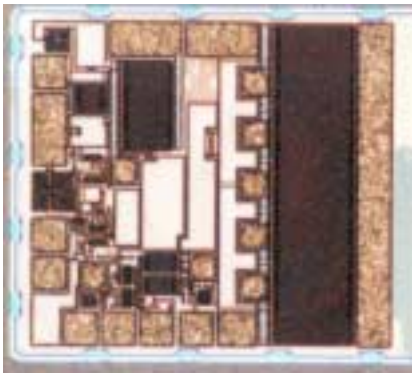

Figure 6. DCS-1800 Layout

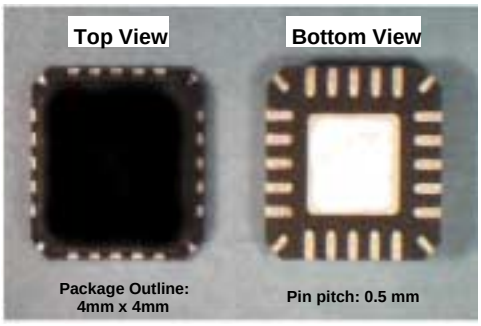

Figure 7. 4mm x 4mm 20 pin package

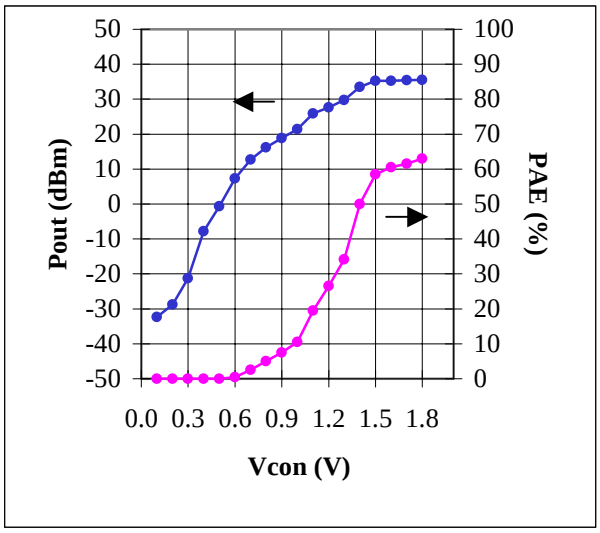

Figure 8. GSM MMIC power control at 900 MHz
Psat=35.5 dBm, PAE=63.0%

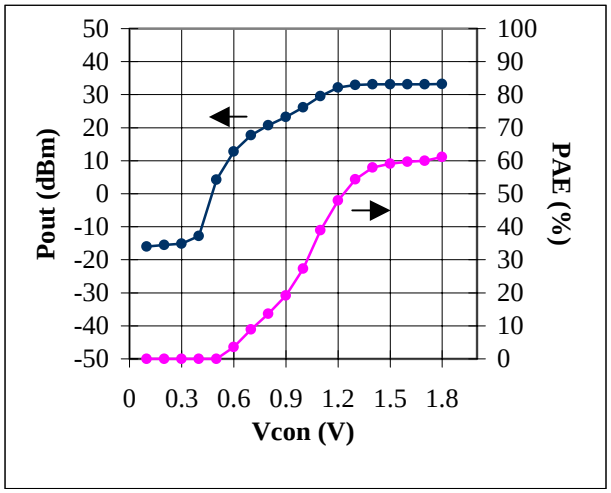

Figure 9. DCS MMIC Power Control at 1750 MHz
Psat=33.2 dBm, PAE=61.1%

V. Conclusion

Two high performance MMICs utilizing the Quasi-Enhancement mode PHEMT technology were presented achieving gradual power control slope, Power Added Efficiencies of 63.0% for GSM and 61.1% for DCS-1800 and adequate output power levels for 3.2V battery voltage operation.

Acknowledgments

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References

[1] T. Moriuchi et al, “A Single Supply Miniature PA MMIC for Multi-mode Digital Handsets using Quasi-Enhancement Mode PHEMT”, IEEE GaAs IC Digest, pp29-32, 2000

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